REMARKS

Claims 1-20 are pending in this application.

Applicant appreciates the Examiner's indication that claims 15-20 are allowed.

Claims 1, 2 and 7-14 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Masanori et al. (EP 0 961 404) in view of Nakamura et al. (U.S. 6,351,196). And claims 3-6 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Masanori et al. in view of Nakamura et al., and further in view of Keiji (EP 0 735 671). Applicant respectfully traverses the rejections of claims 1-14.

Claim 1 recites:

> "A surface acoustic wave apparatus comprising:
> a surface acoustic wave device provided on a piezoelectric substrate, said surface acoustic wave device including at least one interdigital electrode, and **balanced signal terminals provided for at least one of an input side and an output side**;
> a multi-layered retaining substrate including external terminals for connecting the balanced signal terminals to an external device, said multi-layered retaining substrate being provided to retain said surface acoustic wave device such that the at least one interdigital electrode faces a surface of said multi-layered retaining substrate; and
> **an electrical circuit provided between layers of said multi-layered retaining substrate such that said electrical circuit is located between the balanced signal terminals and the external terminals so as to increase a balance degree between the balanced signal terminals**." (emphasis added)

The Examiner alleged that Applicant's arguments with respect to claims 1-14 have been considered but are deemed moot in view of the new grounds of rejection. However, the Examiner has completely failed to address any of the arguments regarding the alleged teachings of Masanori et al. Since the Examiner has again relied upon Masanori et al. to allegedly teach various features recited in the present claimed invention, Applicant respectfully submits that Applicant's arguments with respect to claims 1-14, and specifically with respect to Masanori et al., are **NOT** moot in view of the new grounds of rejection, and were instead, improperly ignored by the Examiner.

Accordingly, Applicant respectfully requests that, the Examiner fully and specifically respond to Applicant's arguments regarding the alleged teachings of Masanori et al.

The Examiner alleged that Masanori et al. teaches all of the features recited in Applicant's claim 1, except for two balanced signal terminals provided for input and output terminals. The Examiner further alleged that Nakamura et al. teaches a piezoelectric substrate 11 having two balanced signal terminals provided for input (IN) and output (OUT) terminals "for the purpose of improving the balance level in the balanced type input and output terminal." Thus, the Examiner concluded that it would have been obvious "to modify Masanori [et al.] surface acoustic wave apparatus with the teaching of Nakamura [et al.] balance signal terminal for the purpose of reducing insertion losses and improving the balance level in the balance type input and output terminal." Applicant respectfully disagrees.

The Examiner alleged that Masanori et al. teaches a multi-layer retaining substrate (104, 104c) in Fig. 26, and an electrical circuit (P2) in Fig. 20 provided between the layers of the multi-layer substrate. This is clearly incorrect. Contrary to the Examiner's allegations, Masanori et al. clearly fails to teach or suggest the features of "an electrical circuit provided between layers of said multi-layered retaining substrate such that said electrical circuit is located between the balanced signal terminals and the external terminals so as to increase a balance degree between the balanced signal terminals" as recited in Applicant's claim 1.

Masanori et al. discloses, in col. 19, lines 9-14, that "referring to FIG. 26, the SAW-filter package device 100C uses a bottom plate 104C in the package body 12 **in place of the bottom plate 104**" (emphasis added), not that the bottom plates are used together to define a multi-layered substrate, as alleged by the Examiner. Thus, contrary to the Examiner's allegation, neither of bottom plate 104 and bottom plate 104C can be fairly construed as a multi-layered retaining substrate. At best, Masanori et al. merely teaches a bottom plate which includes **only a single layer**.

The Examiner further alleged that element P2 of Masanori et al. is an electrical

circuit. However, element P2 of Masanori et al. is specifically disclosed as being a **printed circuit board**, **NOT** an **electrical circuit**.

In addition, the Examiner alleged that element P2 of Masanori et al. is located between the balanced signal terminals (20, 46) and the external terminals (113, 116) to increase the balance degree between the balanced signal terminals. However, contrary to the Examiner's allegation, Masanori et al. fails to teach or suggest anything at all about the specific location and arrangement of printed circuit board P2, and certainly fails to teach or suggest an electrical circuit that is arranged as recited in Applicant's claim 1.

Furthermore, contrary to the Examiner's allegation, Masanori et al. fails to teach or suggest that the printed circuit board P2 increases a balance degree between balanced signal terminals. In fact, Masanori et al. fails to teach or suggest any specific element or structure which is provided so as to increase a balance degree between balanced signal terminals, or even that the balance degree between balanced signal terminals could or should be increased.

Instead of basing the conclusion of obviousness on actual teachings or suggestions of the prior art and the knowledge of one of ordinary skill in the art at the time the invention was made, the Examiner has improperly used Applicant's own invention as a guide. It is impermissible to use the claimed invention as an instruction manual or 'template' to piece together the teachings of the prior art so that the claimed invention is rendered obvious. This court has previously stated that one cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention. In re Fritch, 972 F.2d 1260, 23 USPQ 2d 1780, 1784 (Fed. Cir. 1992).

Thus, for the reasons described above, Masanori et al. clearly fails to teach or suggest "an electrical circuit provided between layers of said multi-layered retaining substrate such that said electrical circuit is located between the balanced signal terminals and the external terminals so as to increase a balance degree between the

balanced signal terminals" as recited in Applicant's claim 1.

Nakamura et al. was relied upon to allegedly teach two balanced signal terminals provided with an input and output. However, Nakamura et al. clearly fails to teach or suggest "an electrical circuit provided between layers of said multi-layered retaining substrate such that said electrical circuit is located between the balanced signal terminals and the external terminals so as to increase a balance degree between the balanced signal terminals" as recited in Applicant's claim 1.

Keiji is relied upon merely to teach an adjustor 23, and certainly fails to teach or suggest "balanced signal terminals provided for at least one of an input side and an output side" and "an electrical circuit provided between layers of said multi-layered retaining substrate such that said electrical circuit is located between the balanced signal terminals and the external terminals so as to increase a balance degree between the balanced signal terminals" as recited in Applicant's claim 1.

Thus, Applicant respectfully submits that Nakamura et al. and Keiji et al. fail to cure the deficiencies of Masanori et al. described above.

Accordingly, Applicant respectfully submits that Masanori et al., Nakamura et al. and Keiji, applied alone or in combination, fail to teach or suggest the unique combination and arrangement of elements recited in claim 1 of the present application.

In view of the foregoing remarks, Applicant respectfully submits that claim 1 is allowable. Claims 2-14 depend upon claim 1, and are therefore allowable for at least the reasons that claim 1 is allowable. Claims 15-20 are allowed, as indicated by the Examiner.

In view of the foregoing remarks, Applicant respectfully submits that this application is in condition for allowance. Favorable consideration and prompt allowance are solicited.

To the extent necessary, Applicant petitions the Commissioner for a One-month extension of time, extending to December 29, 2003, the period for response to the Office Action dated August 27, 2003.

The Commissioner is authorized to charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-1353.

Respectfully submitted,

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